METHOD AND APPARATUS FOR PACKAGING TEST INTEGRATED CIRCUITS

ABSTRACT OF THE DISCLOSURE

An system IC is partitioned into test ICs that have a sub-set of the functionality of the system IC. The test ICs have chip I/O pads conforming to a sub-set arrangement of the system IC chip I/O pads. A packaging module is designed to accept means for attaching and fanning-out the system IC chip I/O pads to lower density packaging I/O pads. A test IC is electrically coupled to the packaging module and tested by programming signals and power to the signal and power pads on the module packaging I/O pads corresponding to chip I/O pads for the test IC. Functionality of the system IC may be partitioned into a plurality of test ICs, each with chip I/O pads that conform to an individual sub-set of the system IC I/Os. Two or more of the plurality of test ICs are coupled to the system IC packaging module for testing.